## REMARKS

### Present Status of the Application

Claims 1-8 have been withdrawn. The Office Action rejected claims 9-10. Specifically, the Office Action rejected claim 10 under 35 U.S.C. 112 because the limitation "the amorphous silicon layer" is insufficient antecedent basis in the claim. The Office Action also rejected claims 9-10 under 35 U.S.C. 103(a) as being unpatentable over Hamada (U.S. 5,888,856) in view of Miyasaka (U.S. 6,124,154). Applicant has amended claim 10 to overcome the rejection. After entry of the foregoing amendments, claims 9-10 remain pending in the present application, and reconsideratio of those claims is respectfully requested.

### Discussion of Office Action Rejections

The Office Action rejected claim 10 under 35 U.S.C. 112 because the limitation "the amorphous silicon layer" is insufficient antecedent basis in the claim. Applicant amend the limitation of "the amorphous silicon layer" to -the poly-silicon layer- in claim 10 to overcome the rejection. That is described in paragraph [0028] in the specification.

*Applicant respectfully traverses the rejection of claims 9-10 under 103(a) as being unpatentable over Hamada (U.S. 5,888,856) in view of Miyasaka (U.S. 6,124,154) because a prima facie case of obviousness has not been established by the Office Action.*

To establish a prima facie case of obviousness under 35 U.S.C. 103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must

teach or suggest each and every element in the claims. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skilled in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three requirements must " be found in the prior art, and not be based on applicant's disclosure." See M.P.E.P. 2143, 8th ed., February 2003.

The present invention is in general related a low temperature poly-silicon thin film transistor (LTPS TFT) as claim 9 recites:

Claim 9. A low temperature poly-silicon thin film transistor (LTPS TFT), comprising:
***a poly-silicon layer, deposited on a substrate, wherein the height/width ratio of a plurality of mounds on a surface of the poly-silicon layer is less than 0.2,*** and the poly-silicon layer comprises a source, a drain, and a channel that is deposited in between the source and the drain;

a gate isolation layer, deposited on the substrate, and covering the poly-silicon layer;

a gate, correspondingly deposited on the gate isolation layer that is deposited above the channel;

a dielectric layer, deposited on the gate isolation layer, and covering the gate;

a source metal layer, deposited on a surface of the dielectric layer and in the dielectric layer and the gate isolation layer wherein the source metal layer is electrically connected to the source; and

a drain metal layer, deposited on the surface of the dielectric layer and in the dielectric layer and the gate isolation layer wherein the drain metal layer is electrically connected to the drain.

Hamada discloses a top-gate type thin film transistor as shown in FIG. 4I including a substrate 1, a silicon oxide layer 2, a polysilicon layer 3a having a source 31, a drain 32 and a channel 33, a gate oxide layer 4, a gate 5a, and insulating layer 6, electrode layers 7a, 7b

electrically connected with source 31 and drain 32. Hamada fails to teach a height/width ratio of a plurality of mounds on a surface of the polysilicon layer is less than 0.2.

The Office Action points out that in the specification of the claimed invention, having a height/width ratio of a plurality of mounds on a surface of the polysilicon layer is less than 0.2 is not shown as being critical. Applicant provides some photographs as follows to show the height/width ratio of the mounds on the polysilicon layer of the present application is significantly less than that on the polysilicon layer of a conventional TFT.

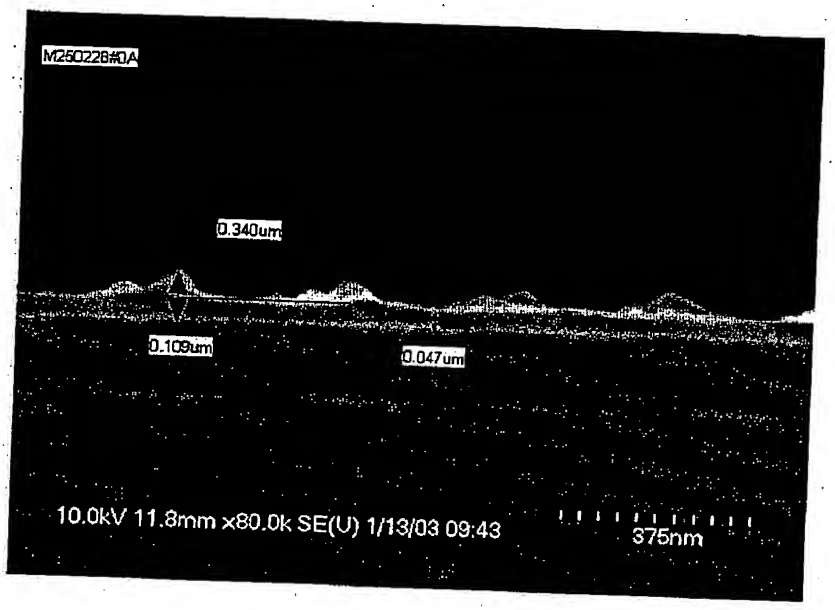


Fig. 1

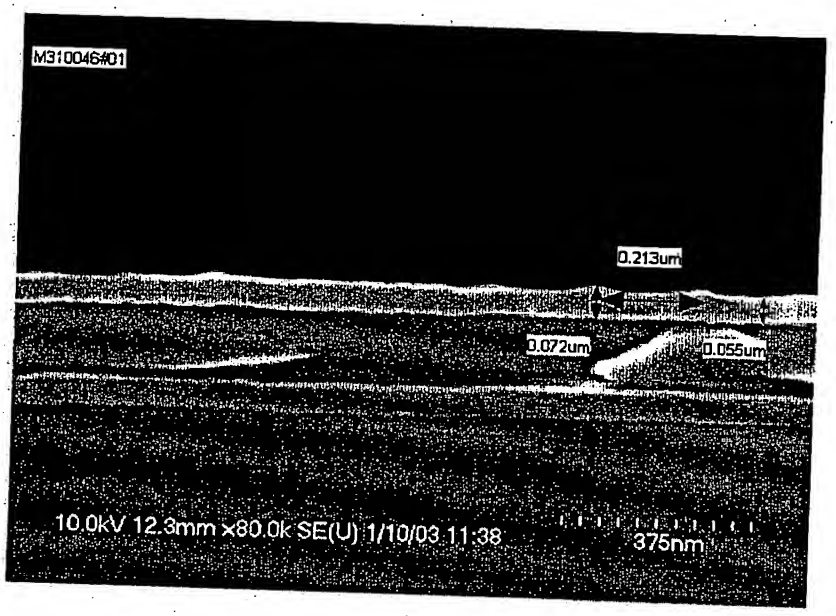


Fig. 2

Fig. 1 shows a polysilicon layer of a conventional TFT, and Fig. 2 shows a polysilicon layer of a TFT of the present invention. Usually, the polysilicon layer of a conventional TFT (as shown in Fig. 1) having a height/width ratio of a plurality of mounds on it surface is about 0.45. It is noted that the mound size on the surface of the polysilicon layer impacts the current characteristic of TFT, especially when the mound size is increased to a certain extent, the current on the TFT is than changed that is described in paragraph [0006] of the specification. In addition, paragraph [0006] of the specification also indicates that if the sizes of the mounds are quite different, the current characteristic of each TFT in display will be not the same, and the display uniformity of the display panel is impacted accordingly. Hence, reducing the

height/width ratio of the mounds and improving the mound size uniformity on the surface of the polysilicon layer is needed.

The Office Action also points out that Miyasaka teaches a laser anneal treatment of a polysilicon layer which improves film surface. However, Applicant submits that Miyasaka just discloses several laser anneal treatments such as melt crystallization, solid phase crystallization (SPC) and very short time-SPC to anneal the amorphous layer. However, Miyasaka does not disclose about the height/width ratio (or the mound size) and the mound uniformity issues, and Miyasaka also does not teach or suggest the height/width ratio of a plurality of mounds on a surface of the polysilicon layer is less than 0.2 for improving the current characteristic of the TFT.

For at least the foregoing reasons, Applicant respectfully submits that independent claim 9 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claim 10 patently define over the prior art as well.

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## CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 9-10 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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